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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,451	12/03/2003	Peter J. Hopper	100-18010 (P05268-D01)	7097

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EXAMINER	
LEE, KYOUNG	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,451	HOPPER ET AL.	
	Examiner	Art Unit	
	Kyoung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *65-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *65-80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/06, 4/24/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 65-80 are rejected under 35 U.S.C. 102(e) as being anticipated by Farrar et al. (U.S. Patent Application Publication No. 2002/0024150).

[Re claim 65 and 69] Farrar discloses a method of forming a conductor on a semiconductor structure, the semiconductor structure having a layer of insulation material and a via that contacts the layer of insulation material, the layer of insulation material having a top surface, the method comprising: etching the top surface of the layer of insulation material (55) to form a plurality of spaced-apart first openings (56a) in the top surface of the layer of insulation material, each first opening having a bottom surface that lies below the top surface of the layer of insulation material; and simultaneously etching the top surface of the layer of insulation material and the bottom surface of each first opening to form a second opening (65) in the top surface of the layer of insulation material, and lower the bottom surface of each first opening to form a plurality of spaced-apart lowered first openings that expose the via or contact, the

second opening having a top that lies in a common plane with the top surface of the layer of insulation material and includes no portion of the top surface of the layer of insulation material, and a bottom that lies below the top surface of the layer of insulation material, each of the plurality of spaced-apart lowered first openings extending away from the bottom of the second opening (see figure 10-13 and paragraph [0050]-[0051]).

[Re claim 66, 67, 70, and 71] Farrar also discloses the method wherein the bottom surface of each lowered first opening exposes an area of the via or contact and an area of the insulation material, the area of the insulation material that is exposed being substantially greater than the area of the via that is exposed (see figure 10-13 and paragraph [0050]-[0051]).

[Re claim 68 and 72] Farrar also discloses the method comprising: depositing a conductive material (80) on the top surface of the layer of insulation material to fill up the second opening and the plurality of spaced-apart lowered first openings; and removing the conductive material from the top surface of the layer of insulation material so that a top surface of the conductive material and the top surface of the insulation region lie approximately in a common plane to form a conductive region, the conductive region having a first region that lies in the second opening, and a plurality of spaced-apart second regions that lies in the plurality of spaced-apart lowered first openings to extend away from the first region, each second region contacting the via or contact (see figures 14-15 and paragraph [0052]-[0053].

[Re claim 73] Farrar discloses a method of forming a conductive line on a semiconductor structure, the semiconductor structure having a layer of insulation

material, the layer of insulation material having a top surface, the method comprising: etching the top surface of the layer of insulation material (55) to form a plurality of spaced-apart first trenches (56a) in the top surface of the layer of insulation material, each first trench having a bottom surface that lies below the top surface of the layer of insulation material, a first width, and a first length that is substantially greater than the first width; and simultaneously etching the top surface of the layer of insulation material and the bottom surface of each first trench to form a second trench (65) in the top surface of the layer of insulation material, and lower the bottom surface of each first trench to form a plurality of spaced-apart lowered first trenches, the second trench having a top that lies in a common plane with the top surface of the layer of insulation material and includes no portion of the top surface of the layer of insulation material, a bottom that lies below the top surface of the layer of insulation material, a second width, and a second length that is substantially greater than the second width, each of the plurality of spaced-apart lowered first trenches extending away from the bottom of the second trench and having a third width and a third length that is substantially greater than the third width (see figure 10-13 and paragraph [0050]-[0051]).

[Re claim 74] Farrar also discloses the method wherein the plurality of spaced-apart lowered first trenches lie substantially parallel to each other (see figures 10-11).

[Re claim 75] Farrar also discloses the method wherein the second and third lengths are approximately equal (see figures 10-13).

[Re claim 76] Farrar also discloses the method comprising: depositing a conductive material (80) on the top surface of the layer of insulation material to fill up

the second trench and the plurality of spaced-apart lowered first trenches; and removing the conductive material from the top surface of the layer of insulation material so that a top surface of the conductive material and the top surface of the insulation region lie substantially in a common plane to form a conductive trace, the conductive trace having a first region that lies in the second trench, and a plurality of spaced-apart second regions that lies in the plurality of spaced-apart lowered first trenches to extend away from the first region (see figures 14-15 and paragraph [0052]-[0053].

[Re claim 77] Farrar also discloses the method wherein the conductive trace is formed to have a number of loops that lie substantially in a same plane (see figure 15 and paragraph [0053]).

[Re claim 78 and 79] Farrar also discloses the method wherein the bottom surface of each lowered first trench exposes an area of a conductive region and an area of the insulation material, the area of the insulation material that is exposed being substantially greater than the area of the conductive region that is exposed (see figure 13 and paragraph [0050]-[0051]).

[Re claim 80] Farrar also discloses the method wherein the second trench has an approximately uniform width (see figure 13).

Response to Amendment

The arguments filed on 4/14/2006 under 37 CFR 1.131 are sufficient to overcome the Tseng (U.S. Patent No. 5,741,741) reference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyoung Lee whose telephone number is (571) 272-1982. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KL 7/5/06

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER